NATIONAL BOARD OF ACCREDITATION

Data Capturing Points of the Program Applied for NBA Accreditation– Tier I/II UG (Engineering) Institute Programs

Program Name : Electronics & Communication Engineering	**Discipline**: Engineering & Technology
Level : Under Graduate	**Tier**: 1
Application No: 10318	**Date of Submission**: 15-03-2025

PART A- Profile of the Institute

A1.Name of the Institute: MLR INSTITUTE OF TECHNOLOGY	
Year of Establishment : 2005	Location of the Institute: Dundigal
A2. Institute Address:NA	
City:--Select--	State:Andhra Pradesh
Pin Code:500043	Website:www.mlrit.ac.in
Email:DIRECTOR@MLRINSTITUTIONS.AC.IN	Phone No(with STD Code):99-49810842
A3. Name and Address of the Affiliating University (if any):	
Name of the University : JNT UNIVERSITY HYDERABAD	City: Medchal
State : Telangana	Pin Code: 500085
A4. Type of the Institution: Self-Supported Institute	
A5. Ownership Status: Self financing	

A6. Details of all Programs being Offered by the Institution:

- No. of UG programs: **11**
- No. of PG programs: **5**

Table No. A6.1: List of all programs offered by the Institute.

Sr.No.	Discipline	Level of program	Name of the program	Year of Start	Year of Closed	Name of The Department
1	Engineering & Technology	UG	Aeronautical Engineering	2005	--	Aeronautical Engineering
2	Engineering & Technology	PG	Aerospace Engineering	2010	2024	Aeronautical Engineering
3	Engineering & Technology	UG	Artificial Intelligence and Machine Learning	2021	2022	Artificial Intelligence and Machine Learning
4	Engineering & Technology	UG	Computer Science & Information Technology	2020	2024	Computer Science and Information Technology
5	Engineering & Technology	UG	Computer Science and Engineering	2005	--	Computer Science and Engineering
6	Engineering & Technology	PG	Computer Science and Engineering	2011	--	Computer Science and Engineering
7	Engineering & Technology	UG	Computer Science and Engineering (Artificial Intelligence & Machine Learning)	2020	--	Computer Science and Engineering (Artificial Intelligence and Machine Learning)
8	Engineering & Technology	UG	Computer Science and Engineering (Cyber Security)	2020	2023	Computer Science and Engineering (Cyber Security)

9	Engineering & Technology	UG	Computer Science and Engineering (Data Science)	2020	--	Computer Science and Engineering (Data Science)
10	Engineering & Technology	UG	Electrical & Electronics Engineering	2017	--	Electrical and Electronics Engineering
11	Engineering & Technology	UG	Electronics & Communication Engineering	2005	--	Electronics and Communication Engineering
12	Engineering & Technology	PG	Embedded Systems	2014	--	Electronics and Communication Engineering
13	Engineering & Technology	UG	Information Technology	2005	2024	Information Technology
14	Engineering & Technology	UG	Mechanical Engineering	2009	--	Mechanical Engineering
15	Engineering & Technology	PG	Thermal Engineering	2013	--	Mechanical Engineering
16	Management	PG	Master of Business Administration	2006	--	Management

A7. Programs to be considered for Accreditation vide this Application:

Table No. A7.1: List of programs to be considered for accreditation.

Name of the Department	Having Allied Departments	Name of the Program	Program Level
Aeronautical Engineering	No	Aeronautical Engineering	UG
Mechanical Engineering	No	Mechanical Engineering	UG
Computer Science and Engineering	Yes	Computer Science and Engineering	UG
Electronics and Communication Engineering	No	Electronics & Communication Engineering	UG

Table No. A7.2: Allied Department(s) to the Department of the program considered for accreditation as above.

Cluster ID. Name of the Department (in table no. A7.1) Name of allied Departments/Cluster (for table no. A7.1)

No Record

PART-B: Program information

B1. Provide the Required Information for the Program Applied For:

Table No. B1: Program details.

A. List of the Programs Offered by the Department:

SR.NO.	PROGRAM NAME	PROGRAM APPLIED LEVEL	YEAR OF START / YEAR OF CLOSED	SANCTIONED INTAKE	INCREASE/DECREASE INTAKE (if any)	YEAR OF INCREASE/DECREASE	CURRENT INTAKE	YEAR OF AICTE APPROVAL	AICTE/COMPETENT AUTHORITY ARROVAL DETAILS	ACCREDITATION STATUS	FROM	TO	NO. OF TIMES PROGRAM ACCREDITED	PROGRAM DURATION
1	Electronics & Communication Engineering	UG	2005 / --	60	Yes	2024	120	2024	South-Central/1-43665188846/2024/EOA	Granted accreditation for 3 years for the period (specify period)	2016	2025	3	4

SR.NO.	PROGRAM NAME	PROGRAM APPLIED LEVEL	YEAR OF START / YEAR OF CLOSED	SANCTIONED INTAKE	INCREASE/DECREASE INTAKE (if any)	YEAR OF INCREASE/DECREASE	CURRENT INTAKE	YEAR OF AICTE APPROVAL	AICTE/COMPETENT AUTHORITY ARROVAL DETAILS	ACCREDITATION STATUS	FROM	TO	NO. OF TIMES PROGRAM ACCREDITED	PROGRAM DURATION

Sanctioned Intake for Last Five Years for the Embedded Systems	
Academic Year	**Sanctioned Intake**
2024-25	120
2023-24	240
2022-23	240
2021-22	240
2020-21	240
2019-20	240

List of the Allied Departments/Cluster and Programs:

B2. Detail of Head of the Department for the program under consideration:

A. Name of the HoD :	Dr. SVS. Prasad
B. Nature of appointment:	Regular
C. Qualification:	ME/M. Tech and PhD

B3. Program Details

Table No.B3.1: Admission details for the program excluding those admitted through multiple entry and exit points.

Item (Information to be provided cumulatively for all the shifts with explicit headings, wherever applicable)	2024-25 (CAY)	2023-24 (CAYm1)	2022-23 (CAYm2)	2021-22 (CAYm3)	2020-21 (CAYm4)	2019-20 (CAYm5)	2018-19 (CAYm6)
N=Sanctioned intake of the program (as per AICTE /Competent authority)	120	240	240	240	240	240	240
N1=Total no. of students admitted in the 1st year minus the no. of students, who migrated to other programs/ institutions plus no. of students, who migrated to this program	120	240	240	240	240	240	240
N2=Number of students admitted in 2nd year in the same batch via lateral entry including leftover seats	0	27	26	27	24	24	24
N3=Separate division if any	0	0	0	0	0	0	0
N4=Total no. of students admitted in the 1st year via all supernumerary quotas	8	15	16	18	0	0	0
Total number of students admitted in the program (N1 + N2 + N3 + N4) - excluding those admitted through multiple entry and exit points.	128	282	282	285	264	264	264

CAY= Current Academic Year. CAYm1= Current Academic Year Minus 1 CAYm2= Current Academic Year Minus 2. LYG= Last Year Graduate. LYGm1= Last Year Graduate Minus 1. LYGm2= Last Year Graduate Minus 2.

B4. Enrolment Ratio in the First Year

Table No. B4.1: Student enrolment ratio in the 1st year.

Year of entry	N (From Table 4.1)	N1 (From Table 4.1)	N4 (From Table 4.1)	Enrollment Ratio [(N1/N)*100]

2024-25 (CAY)	120	120	8	106.67
2023-24 (CAYm1)	240	240	15	106.25
2022-23 (CAYm2)	240	240	16	106.67

Average [(ER1 + ER2 + ER3) / 3] = 106.53≡ 100

B5. Success Rate of the Students in the Stipulated Period of the Program

Table No.B5.1: The success rate in the stipulated period of a program.

Item	(2020-21) LYG	(2019-20) LYGm1	(2018-19) LYGm2
A*= (No. of students admitted in the 1st year of that batch and those actually admitted in the 2nd year via lateral entry, plus the number of students admitted through multiple entry (if any) and separate division if applicable, minus the number of students who exited through multiple entry (if any).	264.00	264.00	264.00
B=No. of students who graduated from the program in the stipulated course duration	244.00	249.00	258.00
Success Rate (SR)= (B/A) * 100	92.42	94.32	97.73

Average SR of three batches ((SR_1+ SR_2+ SR_3)/3): 94.82

B6. Academic Performance of the First-Year Students of the Program

Table No.B6.1: Academic Performance of the First-Year Students of the Program.

Academic Performance	CAYm1(2023-24)	CAYm2(2022-23)	CAYm3 (2021-22)
Mean of CGPA or mean percentage of all successful students(X)	6.69	6.85	6.52
Y=Total no. of successful students	248.00	250.00	257.00
Z=Total no. of students appeared in the examination	255.00	256.00	258.00
API [X*(Y/Z)]	6.51	6.69	6.49

Average API[(AP1+AP2+AP3)/3] : 6.56

B7: Academic Performance of the Second Year Students of the Program

Table No.B7.1: Academic Performance of the Second Year Students of the Program.

Academic Performance	CAYm1 (2023-24)	CAYm2 (2022-23)	CAYm3 (2021-22)
X=(Mean of 2nd year grade point average of all successful students on a 10-point scale) or (Mean of the percentage of marks of all successful students in 2rd year/10)	6.92	6.05	6.00
Y=Total no. of successful students	268.00	272.00	260.00
Z=Total no. of students appeared in the examination	276.00	284.00	262.00
API [X * (Y/Z)]	6.72	5.79	5.95

Average API [(AP1 + AP2 + AP3)/3] : 6.15

B8. Academic Performance of the Third Year Students of the Program

Table No.B8.1: Academic Performance of the Third Year Students of the Program

Academic Performance	CAYm1 (2023-24)	CAYm2 (2022-23)	CAYm3 (2021-22)
X=(Mean of 3rd year grade point average of all successful students on a 10-point scale) or (Mean of the percentage of marks of all successful students in 3rd year/10)	6.97	6.93	6.87
Y=Total no. of successful students	269.00	247.00	253.00

Z=Total no. of students appeared in the examination	272.00	260.00	254.00
API [X*(Y/Z)]:	6.89	6.58	6.84

Average API [(AP1 + AP2 + AP3)/3] : 6.77

B9. Placement, Higher Studies, and Entrepreneurship

Table No.B9.1: Placement, higher studies, and entrepreneurship details.

Item	LYG (2020-21)	LYGm1(2019-20)	LYGm2(2018-19)
FS*=Total no. of final year students	264.00	264.00	264.00
X=No. of students placed	138.00	141.00	149.00
Y=No. of students admitted to higher studies	18.00	47.00	52.00
Z= No. of students taking up entrepreneurship	1.00	1.00	1.00
Placement Index(P) = (((X + Y + Z)/FS) * 100):	59.47	71.59	76.52

Average Placement Index = (P_1 + P_2 + P_3)/3: 69.19 Placement Index Points:

PART C: Faculty Details in Department and Allied Departments

(Data to be filled in for the Department and Allied Departments)

C1. Faculty details of Department and Allied Departments

Table No.C1: Faculty details in the Department for the past 3 years including CAY

Sr.No	Name of the Faculty	PAN No.	Highest degree	University	Area of Specialization	Date of Joining in this Institution	Experience in years in current institute	Designation at Time Joining in this Institution	Present Designation	The date on which Designated as Professor/ Associate Professor if any	Nature of Association (Regular/ Contract/ Ad hoc)	Currently Associated (Y/N)	In case of NO, Date of Leaving	IS HOD?
1	Dr. SVS. Prasad	XXXXXXX26G	XXXXXXXXXXXXXXXPhD	JNTUH	Image processing	02/12/2008	16.2	Associate Professor	Professor	27/11/2017	Regular	Yes		Yes
2	Dr. Sridhar	XXXXXXX28L	XXXXXXXXXXXXXXXPhD	Anna University	Image processing	02/01/2015	10.1	Associate Professor	Professor	02/01/2017	Regular	Yes		No
3	Dr. T.S. Arulananth	XXXXXXX80G	XXXXXXXXXXXXXXXPhD	Dr.MGR Educational &Research Institute	Image processing	05/11/2015	9.3	Associate Professor	Professor	05/07/2016	Regular	Yes		No
4	Dr.Rajan Singh	XXXXXXX90D	XXXXXXXXXXXXXXXPhD	NIT Silchar	VLSI	04/07/2022	2.7	Associate Professor	Professor	15/07/2024	Regular	Yes		No
5	Dr.Md.Moyed Ahmed	XXXXXXX59J	XXXXXXXXXXXXXXXPhD	JNTUH	VLSI	27/12/2021	1.4	Professor	Professor		Regular	No	20/05/2023	No
6	Dr. P.Yakaiah	XXXXXXX98H	XXXXXXXXXXXXXXXPhD	Rayalaseema University	Image processing	18/06/2008	16.8	Assistant Professor	Associate Professor	10/08/2024	Regular	Yes		No

7	Dr. T. Vijetha	XXXXXXX12H	XXXXXXXXXXXXXXXPhD	Osmania University	RF and MWE	13/06/2014	10.8	Assistant Professor	Associate Professor	10/08/2024	Regular	Yes		No
8	Dr.K. NishanthRao	XXXXXXX05L	XXXXXXXXXXXXXXXPhD	Dayananda Sagar university	Antenna with IoT	17/06/2014	10.8	Assistant Professor	Associate Professor	20/07/2023	Regular	Yes		No
9	Dr. Kiran Chand Ravi	XXXXXXX76N	XXXXXXXXXXXXXXXPhD	VIT-AP Univeristy	RF and MWE	06/04/2023	1.10	Associate Professor	Associate Professor	06/04/2023	Regular	Yes		No
10	Dr. D.Laxma Reddy	XXXXXXX23B	XXXXXXXXXXXXXXXPhD	Dayananda Sagar university	Wireless Communication	06/06/2013	11.8	Assistant Professor	Associate Professor	10/07/2023	Regular	Yes		No
11	Dr. G.Karthik Reddy	XXXXXXX36G	XXXXXXXXXXXXXXXPhD	Osmania University	Wireless networks	12/04/2013	11.10	Assistant Professor	Associate Professor	10/08/2022	Regular	Yes		No
12	Dr. K. Phaneendra	XXXXXXX74R	XXXXXXXXXXXXXXXPhD	JNTUK	Speech Signal Processing	13/02/2023	2	Associate Professor	Associate Professor	13/02/2023	Regular	Yes		No
13	Dr. Srikanth Upadhyay	XXXXXXX38L	XXXXXXXXXXXXXXXPhD	Jaipur University	Signal Processing	14/02/2024	1	Associate Professor	Associate Professor	14/02/2024	Regular	Yes		No
14	Dr.Ramkrishna Sharma	XXXXXXX28J	XXXXXXXXXXXXXXXPhD	JNTU	Wireless Mobile Communications	18/01/2024	1.1	Associate Professor	Associate Professor	18/01/2024	Regular	Yes		No
15	Dr.Pulkit singh	XXXXXXX23E	XXXXXXXXXXXXXXXPhD	NIT, Rayapur	VLSI	11/07/2022	2.7	Assistant Professor	Associate Professor	21/08/2024	Regular	Yes		No
16	Dr. G.V.S Manoj Kumar	XXXXXXX17H	XXXXXXXXXXXXXXXPhD	Dr.MGR Educational &Research Institute	VLSI & ES	24/06/2022	2.8	Assistant Professor	Associate Professor	10/07/2024	Regular	Yes		No
17	Dr. Sudeep Sharma	XXXXXXX68H	XXXXXXXXXXXXXXXPhD	JNTU	System Identification	01/10/2021	3	Assistant Professor	Associate Professor	10/08/2022	Regular	No	07/10/2024	No
18	Dr. T.Maddileti	XXXXXXX23A	XXXXXXXXXXXXXXXPhD	JNTUH	VLSI System Design	06/01/2022	1.5	Associate Professor	Associate Professor	06/01/2022	Regular	No	08/06/2023	No
19	Dr. Banoth Ravi	XXXXXXX11J	XXXXXXXXXXXXXXXPhD	IIT, Dhanbad	Wireless Networks	06/07/2022	1.11	Associate Professor	Associate Professor	06/07/2022	Regular	No	11/06/2024	No
20	Dr. Kiran Dasari	XXXXXXX08A	XXXXXXXXXXXXXXXPhD	NIT, Warangal	EMBEDDED SSYTEMS	01/11/2021	2.7	Assistant Professor	Associate Professor	09/08/2023	Regular	No	24/06/2024	No
21	Dr. Manoj Kumar	XXXXXXX55N	XXXXXXXXXXXXXXXPhD	IIT, Dhanbad	Thinfilm Semiconductors	14/07/2022	2.7	Assistant Professor	Assistant Professor		Regular	Yes		No
22	Dr.Y. Siva rama krishna	XXXXXXX34K	XXXXXXXXXXXXXXXPhD	VIT University	SPEECH ENHANCEMENT	01/12/2023	1.2	Assistant Professor	Assistant Professor		Regular	Yes		No
23	Dr. M. Ganesh	XXXXXXX76C	XXXXXXXXXXXXXXXPhD	NIT, Warangal	Wireless Communications	01/09/2023	1.5	Assistant Professor	Assistant Professor		Regular	Yes		No
24	Dr. Bittu Kumar	XXXXXXX28G	XXXXXXXXXXXXXXXPhD	IIT, Dhanbad	Signal Processing	08/07/2022	2.2	Assistant Professor	Assistant Professor		Regular	No	07/09/2024	No
25	Dr. V. Vijay Kumar	XXXXXXX45L	XXXXXXXXXXXXXXXPhD	VIT , University	Medical Image Processing	11/09/2023	1.5	Assistant Professor	Assistant Professor		Regular	Yes		No

26	Mr.K.Haribabu	XXXXXXX34G	M.E/M.Tech	JNTUK	DESC	07/12/2012	12.2	Assistant Professor	Assistant Professor		Regular	Yes		No
27	Mr. V.ShyamBabu	XXXXXXX11G	M.E/M.Tech	JNTUK	DECS	16/11/2015	9.3	Assistant Professor	Assistant Professor		Regular	Yes		No
28	Mr. Ch. Babaiah	XXXXXXX25G	M.E/M.Tech	JNTUH	EMBEDDED SSYTEMS	02/12/2014	10.2	Assistant Professor	Assistant Professor		Regular	Yes		No
29	Mr. R. Sateesh	XXXXXXX24F	M.E/M.Tech	JNTUH	Speech Signal Processing	05/12/2016	8.2	Assistant Professor	Assistant Professor		Regular	Yes		No
30	Mr. A. Sudhakar	XXXXXXX56E	M.E/M.Tech	JNTUH	EMBEDDED SSYTEMS	10/11/2015	9.3	Assistant Professor	Assistant Professor		Regular	Yes		No
31	Mr. K. Mani Raj	XXXXXXX44F	M.E/M.Tech	JNTUH	EMBEDDED SSYTEMS	04/02/2015	10	Assistant Professor	Assistant Professor		Regular	Yes		No
32	Mr. M. RajuNaik	XXXXXXX97D	M.E/M.Tech	JNTUH	EMBEDDED SSYTEMS	15/06/2016	8.8	Assistant Professor	Assistant Professor		Regular	Yes		No
33	Mrs. Y. Geetha	XXXXXXX68L	M.E/M.Tech	JNTUH	EMBEDDED SSYTEMS	25/07/2017	7.6	Assistant Professor	Assistant Professor		Regular	Yes		No
34	Ms. B. Anusha	XXXXXXX81R	M.E/M.Tech	JNTUH	VLSI	05/12/2017	7.2	Assistant Professor	Assistant Professor		Regular	Yes		No
35	Ms. B. Sirisha	XXXXXXX18B	M.E/M.Tech	JNTUH	DECS	09/03/2023	1.11	Assistant Professor	Assistant Professor		Regular	Yes		No
36	Mrs. K.Durga Sowjanya	XXXXXXX56F	M.E/M.Tech	JNTUK	EMBEDDED SSYTEMS	18/11/2015	9.3	Assistant Professor	Assistant Professor		Regular	Yes		No
37	Mrs.P.Sahithya	XXXXXXX78N	M.E/M.Tech	JNTUK	VLSI & ES	11/06/2022	2.8	Assistant Professor	Assistant Professor		Regular	Yes		No
38	Mr. G Kaushik	XXXXXXX16A	M.E/M.Tech	JNTUH	EMBEDDED SSYTEMS	26/08/2019	5.5	Assistant Professor	Assistant Professor		Regular	Yes		No
39	Mrs.N.Poornima Deepthi	XXXXXXX40R	M.E/M.Tech	JNTUH	DECS	12/02/2022	3	Assistant Professor	Assistant Professor		Regular	Yes		No
40	Mrs.Akhila Akula	XXXXXXX59R	M.E/M.Tech	JNTUH	EMBEDDED SSYTEMS	07/12/2022	2.2	Assistant Professor	Assistant Professor		Regular	Yes		No
41	Mr. S. Naveen Kumar	XXXXXXX69P	M.E/M.Tech	JNTUH	SYSTEMS AND SIGNAL PROCESSING	03/07/2023	1.7	Assistant Professor	Assistant Professor		Regular	Yes		No
42	Mr. B. Kiran Kumar	XXXXXXX25Q	M.E/M.Tech	JNTUH	VLSI SYSTEM DESIGN	06/06/2022	2.8	Assistant Professor	Assistant Professor		Regular	Yes		No
43	Mr. L.Sandeep Kumar	XXXXXXX64A	M.E/M.Tech	NIT, Calicut	Telecommunications	19/08/2022	2.6	Assistant Professor	Assistant Professor		Regular	Yes		No
44	Mr.S. Rahul	XXXXXXX37F	M.E/M.Tech	JNTUH	VLSI SYSTEM DESIGN	13/06/2022	2.8	Assistant Professor	Assistant Professor		Regular	Yes		No
45	Ms.K.Mary	XXXXXXX81K	M.E/M.Tech	JNTUH	EMBEDDED SSYTEMS	19/02/2024	1	Assistant Professor	Assistant Professor		Regular	Yes		No

46	Mr.V. Arun Kumar	XXXXXXX73K	M.E/M.Tech	JNTUH	DECS	18/04/2023	1.10	Assistant Professor	Assistant Professor		Regular	Yes		No
47	Mr.K.Pithamber	XXXXXXX76M	M.E/M.Tech	JNTUH	VLSI	19/02/2024	1	Assistant Professor	Assistant Professor		Regular	Yes		No
48	Mr. K.Purushotham	XXXXXXX17A	M.E/M.Tech	JNTUH	Wireless Communication	20/02/2024	0.11	Assistant Professor	Assistant Professor		Regular	Yes		No
49	Mrs.S.Monika	XXXXXXX30M	M.E/M.Tech	JNTUH	EMBEDDED SSYTEMS	13/09/2017	7.5	Assistant Professor	Assistant Professor		Regular	Yes		No
50	Mrs. M.Sailaja	XXXXXXX74K	M.E/M.Tech	JNTUH	CMCS	04/12/2017	7.2	Assistant Professor	Assistant Professor		Regular	Yes		No
51	Mr. P.Ramesh	XXXXXXX28J	M.E/M.Tech	JNTUH	DCS	15/05/2012	12.9	Assistant Professor	Assistant Professor		Regular	Yes		No
52	Mr. R.Raju	XXXXXXX32P	M.E/M.Tech	JNTUH	DSCE	14/07/2022	2.7	Assistant Professor	Assistant Professor		Regular	Yes		No
53	Mr. M. Nagendra Babu	XXXXXXX96A	M.E/M.Tech	JNTUH	DECS	01/07/2022	2.7	Assistant Professor	Assistant Professor		Regular	Yes		No
54	Mr. Ashok Kumar Cheeli	XXXXXXX66K	M.E/M.Tech	NITK(Suratkal)	Industrial Electronics	07/01/2019	6.1	Assistant Professor	Assistant Professor		Regular	Yes		No
55	Ms. K. Jyothi	XXXXXXX49Q	M.E/M.Tech	JNTUH	DSCE	30/11/2016	7.5	Assistant Professor	Assistant Professor		Regular	No	25/05/2024	No
56	Mr. D. Srikar	XXXXXXX69R	M.E/M.Tech	JNTUH	VLSI	01/02/2020	4.4	Assistant Professor	Assistant Professor		Regular	No	29/06/2024	No
57	Mrs. K. Harika	XXXXXXX92L	M.E/M.Tech	JNTUH	EMBEDDED SSYTEMS	21/12/2021	2.4	Assistant Professor	Assistant Professor		Regular	No	15/05/2024	No
58	Mr. K. Rajashekar	XXXXXXX13H	M.E/M.Tech	JNTUH	CN&S	27/01/2022	2.4	Assistant Professor	Assistant Professor		Regular	No	18/06/2024	No
59	Mr. K. Naveen	XXXXXXX56D	M.E/M.Tech	JNTUH	VLSI	16/11/2015	8.7	Assistant Professor	Assistant Professor		Regular	No	12/07/2024	No
60	Ms. K. Aruna Manjusha	XXXXXXX20L	M.E/M.Tech	JNTUH	VLSI	01/12/2016	6.6	Assistant Professor	Assistant Professor		Regular	No	29/06/2023	No
61	Mrs. B. Venkata Ramana	XXXXXXX44K	M.E/M.Tech	JNTUH	EMBEDDED SSYTEMS	21/12/2019	3.7	Assistant Professor	Assistant Professor		Regular	No	25/07/2023	No
62	Ms. P. Bhavani	XXXXXXX24L	M.E/M.Tech	JNTUH	DECS	25/01/2022	1.4	Assistant Professor	Assistant Professor		Regular	No	26/06/2023	No
63	Mr.G.Nagesh	XXXXXXX86N	M.E/M.Tech	JNTUH	CS	08/08/2022	0.10	Assistant Professor	Assistant Professor		Regular	No	06/07/2023	No
64	Ms. K. Anithabai	XXXXXXX98D	M.E/M.Tech	JNTUH	VLSI	14/06/2016	7.2	Assistant Professor	Assistant Professor		Regular	No	08/09/2023	No
65	Mrs.T. Anuradha	XXXXXXX83P	M.E/M.Tech	JNTUH	VLSI DESIGN	12/02/2016	7.4	Assistant Professor	Assistant Professor		Regular	No	08/07/2023	No

Table No.C2: Faculty details of Allied Departments for the past 3 years including CAY.

C2. Student-Faculty Ratio (SFR)

No. of UG(Engineering) programs in Department including allied departments/ clusters (UGn):
UG1=1st UG program
UGn=nth UG program
B= No. of Students in UG 2nd year (ST)
C= No. of Students in UG 3rd year (ST)
D= No. of Students in UG 4th year (ST)
No. of PG (Engineering) programs in Department including allied departments/ clusters (PGm):
PG1=1st PG program.
PGm=mth PG program
A= No. of Students in PG 1st year
B= No. of Students in PG 2nd year
Student Faculty Ratio **(SFR)** = S/F
S= No. of students of all programs in the Department including all students of allied departments/clusters.
No. of students (ST)=Sanctioned Intake (SA)+ Actual admitted students via lateral entry including leftover seats (L) if any (limited to 10 % of SA)
Students who admitted under supernumerary quotas (SNQ, EWS, etc) will not be considered in calculating SFR value. Those students are exempted.
F=Total no. of regular or contractual faculty members (Full Time) in the Department, including allied departments/clusters (excluding first year faculty (The faculty members who have a 100% teaching load in the first-year courses)).

No. of UG Programs in the Department1 No. of PG Programs in the Department1

Table No.C2.1: Student-faculty ratio.

Description	**CAY(2024-25)**	**CAYm1 (2023-24)**	**CAYm2 (2022-23)**
UG1.B	264	264	264
UG1.C	264	264	264
UG1.D	264	264	264
UG1: Electronics & Communication Engineering	**792**	**792**	**792**
PG1.A	6	12	12
PG1.B	12	12	18
PG1: Embedded Systems	**18**	**24**	**30**
DS=Total no. of students in all UG and PG programs in the Department	810	816	822
AS=Total no. of students of all UG and PG programs in allied departments	0	0	0
S=Total no. of students in the Department (DS) and allied departments (AS)	**S1=** 810	**S2=** 816	**S3=** 822
DF=Total no. of faculty members in the Department	48	49	51
AF= Total no. of faculty members in the allied Departments	0	0	0
F=Total no. of faculty members in the Department (DF) and allied Departments (AF)	**F1=** 48	**F2=** 49	**F3=** 51
FF=The faculty members in F who have a 100% teaching load in the first-year courses	3	3	3
Student Faculty Ratio (SFR)=S/(F-FF)	**SFR1= 18.00**	**SFR2= 17.74**	**SFR3= 17.13**
Average SFR for 3 years	**SFR= 17.62**		

C3. Faculty Qualification

- Faculty qualification index (FQI) = 2.5 * [(10X +4Y)/RF] where
- X=No. of faculty members with Ph.D. degree or equivalent as per AICTE/UGC norms.
- Y=No. of faculty members with M. Tech. or ME degree or equivalent as per AICTE/ UGC norms.

- RF=No. of required faculty in the Department including allied Departments to adhere to the 20:1 Student-Faculty ratio, with calculations based on both student numbers and faculty requirements as per section C2 of this documents: (RF=S/20).

Table No.C3.1: Faculty qualification.

Year	X	Y	RF	FQ = 2.5 x [(10X + 4Y) / RF)]
2024-25(CAY)	19	29	40.00	19.12
2023-24(CAYm1)	15	34	40.00	17.88
2022-23(CAYm2)	12	39	41.00	16.83

C4. Faculty Cadre Proportion

- Faculty Cadre Proportion is 1(RF1): 2(RF2): 6(RF3)
- RF1= No. of Professors required = 1/9 * No. of Faculty required to comply with 20:1 Student-Faculty ratio based on no. of students (S) as per C2 of this documents:.
- RF2= No. of Associate Professors required = 2/9 * No. of Faculty required to comply with 20:1 Student-Faculty ratio based on no. of students (S) as per section C2 of this documents:.
- RF3= No. of Assistant Professors required = 6/9 * No. of Faculty required to comply with 20:1 Student-Faculty ratio based on no. of students (S) as per section C2 of this documents:.
- Faculty cadre and qualification and experience should be as per AICTE/UGC norms.

Table No.C4.1: Faculty cadre proportion details.

Year	Professors		Associate Professors		Assistant Professors	
	Required RF1	Available AF1	Required RF2	Available AF1	Required RF3	Available AF3
2024-25	4.00	4.00	9.00	11.00	27.00	33.00
2023-24	4.00	3.00	9.00	9.00	27.00	37.00
2022-23	4.00	4.00	9.00	5.00	27.00	42.00
Average	RF1=4.00	AF1=3.67	RF2=9.00	AF2=8.33	RF2=27.00	AF2=37.33

C5. Visiting/Adjunct Faculty/Professor of Practice

Table No. C5.1: List of visiting/adjunct faculty/professor of practice and their teaching and practical loads.

(CAYm1)

S.No	Name of the Person	Designation	Organization	Name of the Course	No. of hours handled
1	A. Bhagavathi Rao	Retd. Scientist- G	DLRL	Radar Systems	54.00

(CAYm2)

(CAYm3)

C6. Academic Research

Table No. C6.1: Faculty publication details.

S.No.	Item	2023-24 (CAYm1)	2022-23 (CAYm2)	2021-22 (CAYm3)
1	No. of peer reviewed journal papers published	25	23	6

2	No. of peer reviewed conference papers published	70	89	11
3	No. of books/book chapters published	24	2	6

C7. Sponsored Research Project

Table No. C7.1: List of sponsored research projects received from external agencies.

(CAYm1)

PI Name	Co-PI names if any	Name of the Dept., where project is sanctioned	Project Title*	Name of the Funding agency	Duration of the project	Amount(Lacs) i.e. 15,25,000=15.25
Dr Balram Y	Dr T S Arulananth	ECE- MLR institute of technoloy	AICTE IDEA LAB IMPLEMENTATION	AICTE	3 YEARS	90.00
						Amount received (Rs.):90.00

(CAYm2)

(CAYm3)

Total Amount (Lacs) Received for the Past 3 Years: 90.00

Note*:

- Only sponsored research projects will be considered. Infrastructure-based projects will not be considered here.

C8. Consultancy Work

Table No. C8.1: List of consultancy projects received from external agencies.

(CAYm1)

PI Name	Co-PI names if any	Name of the Dept., where project is sanctioned	Project Title*	Name of the Funding agency	Duration of the project	Amount(Lacs) i.e. 15,25,000=15.25
Dr S V S Prasasd	Mr K Maniraj	ECE	Design of IGBT board and general purposekit	SUNSEAS TECGH	6 MONTHS	170000.00
						Amount received (Rs.):170000.00

(CAYm2)

PI Name	Co-PI names if any	Name of the Dept., where project is sanctioned	Project Title*	Name of the Funding agency	Duration of the project	Amount(Lacs) i.e. 15,25,000=15.25
Mr P. Yakaiah		ECE	LED Board theft detectors installation	Vidya Enterprises	3 Months	170000.00
Mr P. Yakaiah		ECE	CCTV Networking	Vidya Enterprises	6 Months	220000.00
Mr G V S Manoj kumar		ECE	CCTV Networking	Guptha's silver palace	3 Months	160000.00
Dr B Sridhar		ECE	Installation of electronic display boards	Guptha's silver palace	3 Months	170000.00
Dr T S Arulananth		ECE	Digital SMPS Board design	Access power care systems	6 Months	200000.00
Dr S V S Prasasd		ECE	Design of IGBT board and general purpose ki	SUNSEAS TECGH	6 Months	205000.00
Dr S V S Prasasd		ECE	Design of IGBT board	M/S Square -S Micro systems	6 Months	210000.00
						Amount received (Rs.):1335000.00

(CAYm3)

PI Name	Co-PI names if any	Name of the Dept., where project is sanctioned	Project Title*	Name of the Funding agency	Duration of the project	Amount(Lacs) i.e. 15,25,000=15.25
Dr S V S Prasasd		ECE	Design a SMPS circuit board	Access power care systems	6 Months	97745.00
Dr S V S Prasasd		ECE	Design IGBT board and General Purpose Kits	Sun seas technologies	3 Months	96200.00
Dr. S V S Prasad		ECE	Design IGBT board and General Purpose Kits	Access power care systems	3 Months	80000.00
						Amount received (Rs.):273945.00

Total amount (Lacs) received for the past 3 years: 1778945.00

Note*:

- Only consultancy projects will be considered. Infrastructure-based projects will not be considered here.

C9. Institution Seed Money or Internal Research Grant to its Faculty for Research Work

Table No. C9.1: List of faculty members received seed money or internal research grant from the Institution.

(CAYm1)

Faculty name	Project title/ Support for Activity	Duration of the project	Amount(Lacs) i.e. 15,25,000=15.25	Amount Utilized(Lacs) i.e. 15,25,000=15.25	Outcomes of the project
Dr S V S Prasad	Medical image segmentation	1 year	1.00	1.00	published as research article in SCI-Q1 Peer review Journal Multimedia tools and applications
Dr T S Arulananth	Classification of Paediatric Pneumonia Using Modified DenseNet-121 Deep-Learning	1 year	1.32	1.32	Output of the project/ Supported for the activity is published as research article in SCI-Q1 Peer review Journal (IEEE Access) with IF 3.75
Dr. Manoj Kumar	Impact of Sn-doping on the optoelectronic properties of zinc oxide crystal: DFT approach	1 year	1.00	1.00	Output of the project/ Supported for the activity is published as research article in SCI-Q1 Peer review Journal (Plos One) with IF: 2.75
Dr. Manoj Kumar	Comparative Studies of Single-Channel Speech Enhancement Techniques	8 months	0.60	0.40	Output of the project/ Supported for the activity is published as research article in SCI-Q3 Peer review Journal with IF: 1.3
Dr T S Arulananth	Semantic segmentation	1 year	1.00	1.00	Output of the project/ Supported for the activity is published as research article in SCI-Q1 Peer review Journal (Plos One) with IF: 2.75
Dr B Sridhar	multimedia transmission	1 year	1.00	1.00	Output of the project/ Supported for the activity is published as research article in SCI-Q1 Peer review Journal Multimedia tools and applications
Dr Rajan singh	simulation of T gate	6 months	0.60	0.60	published as research article in SCI-Q1 Peer review Journal
Dr. Kiran Chand Ravi	Automatic Farm Robot for Precise Farming	6 months	0.35	0.35	1. Increased Crop Yield 2. Reduced Labor and Costs 3. Won prizes in competitions 4.published paper in IEEE conference
Mr. Raju Nayak	Winding Machine	6 months	0.43	0.43	1.Consistent and Accurate Winding 2.Saves Time and Labor
			Amount received (Rs.): 7.30		

(CAYm2)

Faculty name	Project title/ Support for Activity	Duration of the project	Amount(Lacs) i.e. 15,25,000=15.25	Amount Utilized(Lacs) i.e. 15,25,000=15.25	Outcomes of the project
Dr. B Sridhar	Bore well rescue system	6 Months	0.50	0.50	1. Safe Child Rescue 2. Reduced Rescue Time 3. Won prizes in competitions
Dr T Vijetha	Reconfigurable MIMO Antenna design	6 Months	0.56	0.56	Antenna implemented for multi band functioning, IEEE paper published
Dr. Manoj Kumar	Experimental investigation and DFT study of tin-oxide	1 year	1.00	1.00	Output of the project/ Supported for the activity is published as research article in SCI-Q1 Peer review Journal (IEEE Access)
Dr T S Arulananth	PCA Based Dimensional Data Reduction and Segmentation for DICOM Images	1 year	1.00	1.00	Output of the project/ Supported for the activity is published as research article in SCI-Q1 Peer review Journal (Neural processing letters)
Dr. SVS Prasad	Emergency alert system	6 months	0.55	0.55	1. Quick Response to Danger 2. Saves Live 3.Published paper in IEEE paper 4. Own prizes in competitions
			Amount received (Rs.): 3.61		

(CAYm3)

Faculty name	Project title/ Support for Activity	Duration of the project	Amount(Lacs) i.e. 15,25,000=15.25	Amount Utilized(Lacs) i.e. 15,25,000=15.25	Outcomes of the project
Dr. SVS Prasad	Implementation of Smart traffic management system	6 Months	0.65	0.65	1. Reduced Traffic Jams 2 Improved Road Safety 34.published paper in IEEE conference
Mr. Raju Nayak	Design of Smart Wheel chair physically challenged people	8 Months	0.75	0.75	1.Easy and Independent Movement 2 Enhanced Safety and Comfort
Dr T S Arulananth	Evaluation of low power consumption network on chip routing architecture	1 year	1.00	1.00	published as research article in SCI-Q1 Peer review Journal Microprocessors and microcontrollers)& M.Tech graduate the student
Dr B Sridhar	Security enhancement in video based on gatefold technique for copyright protection	1 year	1.00	1.00	Output of the project/ Supported for the activity is published as research article in SCI-Q1 Peer review Journal Multimedia tools and applications
			Amount received (Rs.): 3.40		

Total amount (Lacs) received for the past 3 years : 14.31

PART D: Laboratory Infrastructure in the Department

(Data to be filled in for the Department)

D1. Adequate and Well-Equipped Laboratories, and Technical Manpower

Table No.D1.1: List of laboratories and technical manpower.

Sr. No	Name of the Laboratory	Number of students per set up(Batch Size)	Name of the Important Equipment	Weekly utilization status(all the courses for which the lab is utilized)	Technical Manpower Support		
					Name of the Technical staff	Designation	Qualification

1	Analog Circuits Lab / Electronic Devices and Circuits Lab	2	1.General purpose bread board Trainer 2.CRO 3.Decade Inductance Box 4. Function Generators	II year I sem E	Mr.G. SwamyRagaiah	Sr Lab.Asst	DECE
2	Analog And Digital Communications Lab	2	1.1MHz Function generators 1. 2.Dual trace oscilloscopes 3.10MHz Pulse and Data Function	II year II sem E	Mr.G. SwamyRagaiah	Sr Lab.Asst	DECE
3	Basic Simulation Lab	1	1.Computers 2. MATLAB software	II year I sem E	Mr. K.B.K.Prasad	Programmer	B Tech
4	Antennas And Wave Propagation Lab	1	1.Computers 2. ANSYS Software	III year II sem E	Mrs.P.Swetha	Programmer	B Tech
5	Microprocessors And Microcontrollers Lab	1	1. Computers with simulation software 2.ALS-SDA-8086 Microprocessor Trainer Kits 3.ALS-SDA-8051	1. III year I sen	Mr. K.Arun Hrudaynath Re	Lab.Asst	ITI
6	Digital Signal Processing Lab	1	1.Computers with simulation software 2. TMS 320C6713 DSP Processor kits 3. Code Composer	III year II sem E	Mrs. P.Sravani	Programmer	B Tech
7	Data Structures Lab	1	1.Computers 2. Code blocks software	II year I sem E	Mrs.P.Swetha	Programmer	B Tech
8	Object Oriented Programming Lab	1	1.Computers with simulation software	III year I sem E	Mrs R.Hymavathi	Programmer	B Tech
9	Analog And Digital IC Applications Lab	1	1.Analog Discovery Kits 2. Regulated Power Supplies 3. Multisim Software 4.Computers 5. Xilinx Software	III year I sem E	Mr.V.Venkatesham	Sr Lab.Asst	DECE
10	VLSI Design Lab	1	1.Computers 2.Cadence Software	IV year I sem E	Mrs. P.Sravani	Programmer	B Tech
11	Embedded and IOT Lab	1	1.Computer Systems with simulation software 28051 based development boards 4 ARM based development	IV year I sem E	Mr. K.B.K.Prasad	Programmer	B Tech
12	Electronic Devices and Circuits Lab	2	1. General purpose bread board trainer kit include 12v-0v-12v AC supplies 2.Dual trace oscilloscopes	I Year II sem E	Mr.Shrini.Siva Raj	Lab.Asst	ITI
13	Digital System Design Lab	1	1.Analog and Digital bread board Trainer Kit 2.5V and 12V DC supplies 3.Logic indicators 4.Logic level	1. II year II sen	Mr. K.Arun Hrudaynath Re	Lab.Asst	ITI
14	IoT Architecture Lab	1	1.Computers with Arduino IDE 2. ESP32 3.Raspberry Pi 4.NODE MCU ESP8266 5.Bread board 6.Arduino Uno	II year II sem E	Mr.V.Venkatesham	Sr Lab.Asst	DECE

D2. Safety Measures in Laboratories

Table No. D2.1: List of various safety measures in laboratories.

Sr. No	Laboratory Name	Safety Measures
1	Analog Circuits Lab/Analog And Digital Communications Lab	• Fire Alarm Panel • CC Cameras • Fire Extinguishers • Voltage Stabilizer • First Aid Box • Earthling is done

2	Basic Simulation Lab / Antennas And Wave Propagation Lab	• Fire Alarm Panel • CC Cameras • Fire Extinguishers • Voltage Stabilizer • First Aid Box • Earthling is done
3	Analog And Digital Ic Applications Lab	• Fire Alarm Panel • CC Cameras • Fire Extinguishers • Voltage Stabilizer • First Aid Box • Earthling is done
4	Microprocessors And Microcontrollers Lab/ Digital Signal Processing Lab	• Fire Alarm Panel • CC Cameras • Fire Extinguishers • Voltage Stabilizer • First Aid Box • Earthling is done
5	VLSI Design Lab	• Fire Alarm Panel • CC Cameras • Fire Extinguishers • Voltage Stabilizer • First Aid Box • Earthling is done
6	Embedded and IOT Lab	• Fire Alarm Panel • CC Cameras • Fire Extinguishers • Voltage Stabilizer • First Aid Box • Earthling is done
7	IoT Architecture Lab	• Fire Alarm Panel • CC Cameras • Fire Extinguishers • Voltage Stabilizer • First Aid Box • Earthling is done
8	Digital System Design Lab	• Fire Alarm Panel • CC Cameras • Fire Extinguishers • Voltage Stabilizer • First Aid Box • Earthling is done
9	Data Structures Lab/ Object Oriented Programming Lab	• Fire Alarm Panel • CC Cameras • Fire Extinguishers • Voltage Stabilizer • First Aid Box • Earthling is done
10	Electronic Devices and Circuits Lab	• Fire Alarm Panel • CC Cameras • Fire Extinguishers • Voltage Stabilizer • First Aid Box • Earthling is done

D3. Project Laboratory/Research Laboratory

The Project Laboratory serves as a dynamic innovation space where final-year students actively engage in the development of their major projects, while third-year students utilize it for their minor projects. The lab provides access to specialized resources including the Embedded Systems Lab, where students have successfully designed and built custom robotic models. These student-developed robots have not only demonstrated technical creativity but have also earned accolades in various inter-college competitions and technical events.

The Cadence VLSI Design Lab plays a significant role in equipping final-year students with industry-relevant training and design experience, supporting advanced project development in digital design. Similarly, the HFSS-enabled Antenna Lab empowers students to design, simulate, and analyses antenna systems, leading to the publication of technical papers under faculty mentorship.

Faculty members provide continuous support and guidance to students in their project and research endeavors, encouraging innovation and collaboration. Dedicated time slots are assigned exclusively for final-year project work, ensuring focused development and mentorship. The Project Laboratory fosters a research-driven, hands-on learning environment that nurtures creativity, problem-solving, and technical excellence.

Table.7.5.1 List of project laboratory/research laboratory /Centre of Excellence

S. No	Name of the Laboratory	Details	Reason(s) for creating facility	Utilization
1	LabVIEW Academy Lab	1) License version 8.6 2) 30 Systems 3) MyDAQ 4) MyRIO	1) To advance research in signal processing and embedded systems, driving innovation and technological development. 2) To provide opportunities for students and faculty to publish research in reputed journals and contribute to academic knowledge. 3) To organize certification programs and workshops, enhancing skill development and hands-on experience for students and professionals.	This lab is specifically designed for and extensively utilized by II, III, and IV year students to undertake and advance their research projects, providing them with the resources and support needed for innovative work.
2	Embedded systems and Robotics lab	1) License version 2015 2) 30 Systems	1) To drive innovation and technological development by advancing research in signal processing and embedded systems. 2) To create opportunities for students and faculty to publish research in reputed journals, contributing to the growth of academic knowledge. 3) To organize certification programs and workshops, fostering skill development and providing valuable hands-on experience for both students and professionals.	This lab is specifically designed for and extensively utilized by II, III, and IV year students to undertake and advance their research projects, providing them with the resources and support needed for innovative work.

3	ANSYS HFSS Lab	1) License version Ansys HFSS 19.0 2) Systems	1) To drive innovation and research in the fields of RF, microwave engineering, and high-frequency electromagnetic analysis by leveraging the advanced simulation capabilities of ANSYS HFSS. 2) To offer training programs and workshops that enhance practical skills and hands-on experience in high-frequency design and analysis for students and professionals. 3) To foster collaboration between students, faculty, and industry experts, encouraging real-world problem solving and knowledge exchange through HFSS-based design and simulation projects.	This lab is specifically designed for and extensively utilized by II, III, and IV year students to undertake and advance their research projects, providing them with the resources and support needed for innovative work.
4	Cadence Lab	1) Cadence 2) Xilinx ISE 14.4 3) Vivado Design suite 4) Spartan 3 and 3E FPGA/CPLD KITS 5) ZYNQ Boards 6) DELL, Intel core i3 process with 4 GB RAM 7) PCB Machine	1) To provide hands-on experience in digital circuit design and FPGA implementation using advanced tools like Cadence, Xilinx ISE 14.4, and Vivado Design Suite. 2) To enable students to work with Spartan 3 and 3E FPGA/CPLD Kits and ZYNQ boards, fostering practical knowledge in programmable logic devices and embedded systems. 3) To support research and innovation in the field of electronics by providing an environment for designing, simulating, and testing complex digital systems and SoC applications.	This lab is specifically designed for and extensively utilized by II, III, and IV year students to undertake and advance their research projects, providing them with the resources and support needed for innovative work.

To support students in the Project and Centre of Excellence (CoE) Laboratories, faculty coordinators are assigned to each lab. These faculty coordinators actively mentor students, oversee project development activities, and ensure the optimal use of lab resources. They guide students in planning, executing, and presenting their projects, while also encouraging participation in technical events, internships, and research publications. This structured involvement of faculty coordinators fosters innovation, enhances student engagement, and ensures effective monitoring of project-based learning.

The faculty coordinators for the various labs are:

ANSYS HFSS Lab: Dr.T.Vijetha

Embedded Systems and Robotics Lab: Dr. Manoj Kumar

Cadence Lab: Dr.Rajan Singh

LabVIEW Academy Lab: Dr. G.Karthik Reddy

MATLAB Centre of excellence Lab: Dr. T.S.Arulananth

Proof of Utilization:

To demonstrate the active use of the ANSYS HFSS lab, the following project was successfully carried out by students as part of their academic work:

Project Title: Triple band metamaterial inspired antenna for future terahertz (thz)

Description: This project involves the design of a compact triple-band microstrip antenna integrated with metamaterials for terahertz (THz) applications at 430 GHz, 730 GHz, and 904 GHz. Using a polyimide substrate and MTM unit cells, the antenna achieves high gain and efficiency suitable for miniaturized and wearable devices. Simulations using ANSYS HFSS and CST showed excellent performance with gains up to 10.1 dB and efficiency above 90%. The antenna also performed well on human body models, making it suitable for healthcare and sensing applications. This project demonstrates the effective use of the ANSYS HFSS lab for advanced THz antenna research.

Software Used: ANSYS HFSS
Lab Utilized: ANSYS HFSS Simulation Lab
Outcome: The project showcased the lab's capability to handle advanced high-frequency electromagnetic simulations, thereby providing students with practical exposure to real-world RF design challenges.Fig.7.5.1 shows the simulation results of the project.

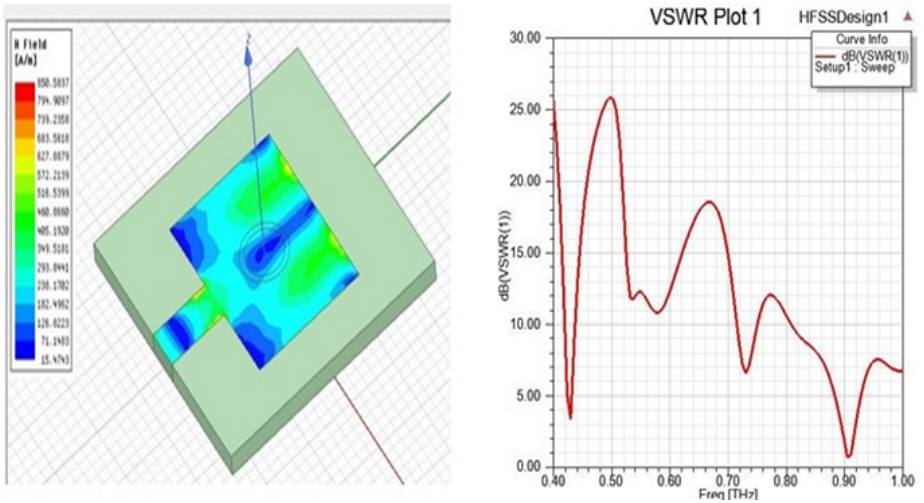

Fig.7.5.1 Simulation results

TRIPLE BAND METAMATERIAL INSPIRED ANTENNA FOR FUTURE TERAHERTZ (THZ)

A

MAJOR PROJECT REPORT

of

Submitted in the Fulfilment of the requirements for the award of the Degree of

BACHELOR OF TECHNOLOGY

IN

ELECTRONICS AND COMMUNICATION ENGINEERING

Submitted by

E. Shashi Kumar	**21R21A0409**
G. Shiva Mani	**21R21A0418**
M. Sai Teja	**21R21A0438**
R. Ajay Kumar	**21R21A0457**

UNDER THE GUIDANCE OF

Mrs. Y. Geetha

(Assistant Professor)

Department of ECE

MARRI LAXMAN REDDY MLR INSTITUTE OF TECHNOLOGY (UGC AUTONOMOUS)

2021-2025

I

Project Title:REALIZATION OF FSM USING CSOC THROUGH ELEVATOR

Description: This Project introduces a new way to design and implement a finite state machine (FSM) using a custom System-on-Chip (SoC) architecture using Verilog HDL. The design takes advantage of the adaptability and effectiveness of custom SoC design to boost the FSMs performance and make the best use of resources. The FSM comes with a mix of hardware and software parts. The hardware components handle critical state transitions, such as emergency stop and floor, while the software components deal with i/o processing and control logic(Verilog Module). The paper explores the design method, drives into implementation specifics of the FPGA design. It shows how this approach drives, including control logic, Verilog code, simulations , synthesis, LUT's Schematics~ for ensuring the potential of elevator's safety and efficiency.

Software Used: Xilinx Vivado Design Suite
Hardware Used: Xilinx FPGA Development Board
Lab Utilized: Xilinx &Vivado FPGA Design Lab

Outcome:
The project demonstrates the effective use of FPGA-based SoC design for real-time embedded control systems. Students gained hands-on experience with Verilog coding, simulation, synthesis, LUT schematic generation, and hardware implementation using Vivado. The solution showcases improved safety and operational efficiency in elevator control systems and reflects the lab's role in fostering practical, industry-relevant skills in digital system design.Fig.7.5.2 Shows the Implemented block digaram.Fig.7.5.3 shows the results.

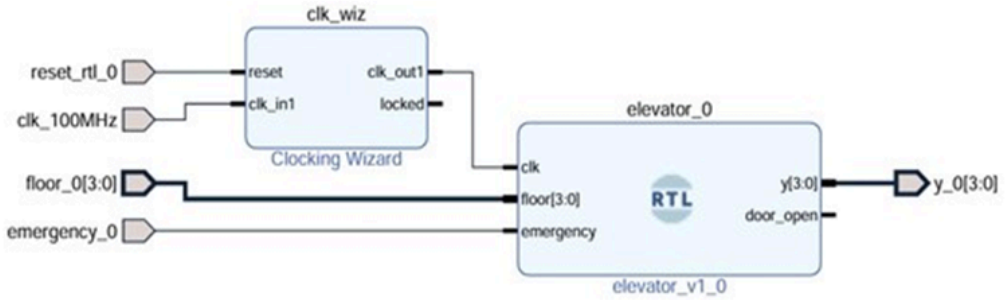

Fig.7.5.2 Implemented Block Design

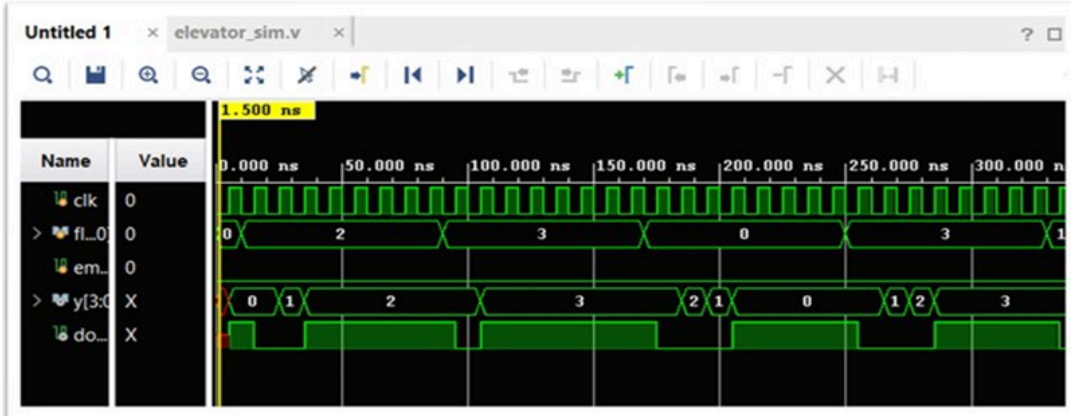

Fig 7.5.3 Simulated O/P without EMERGENCY stop

REALIZATION OF FSM USING CSOC THROUGH ELEVATOR

A

MAJOR PROJECT REPORT

Of

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BACHELOR OF TECHNOLOGY

IN

ELECTRONICS AND COMMUNICATION ENGINEERING

Submitted by

KETHIREDDY SHIVANI

RODDA ARUNA

DEVARAKONDA SHIVA PRASAD

KALAPALA DURGA PRASANNA NAGESHWAR RAO

UNDER GUIDANCE OF

Mrs. N POORNIMA DEEPTHI

(Assistant Professor)

Department of ECE

MARRI LAXMAN REDDY GROUP OF INSTITUTIONS

MLR INSTITUTE OF TECHNOLOGY

(UGC AUTONOMOUS)

Laxman Reddy Avenue, Dundigal, Hyderabad - 500 043, Telangana, India

2021-2025

Project Title:BOREWELL RESCUE ROBOT

Description:
This project addresses the critical issue of bore well accidents, particularly involving children in rural areas. Traditional rescue methods are often time-consuming and risky. The Bore well Rescue Robot is developed to provide a safer, quicker, and more effective alternative. The robot is designed to navigate deep and narrow bore wells and reach the victim with precision.

Equipped with a high-definition camera for real-time video monitoring, a robotic arm for securely grasping the victim, and sensors to monitor environmental parameters like temperature and oxygen levels, the system ensures both situational awareness and safety. Its compact and adaptive mechanical design allows deployment in bore wells of varying diameters and depths.

Software/Hardware Used: Embedded C, Microcontrollers (e.g., Arduino/Raspberry Pi), Motor Drivers, Sensors, Wireless Camera
Lab Utilized: Embedded Systems & Robotics Lab

Outcome:
The project effectively demonstrates the use of embedded systems, robotics, and sensor integration in real-world rescue applications. Students gained practical experience in mechanical design, sensor interfacing, motor control, and real-time monitoring systems. The robot serves as a functional prototype that can be further developed into a deployable solution for emergency rescue missions in bore well accidents.Fig.7.5.4 & Fig.7.5.5 shows results of the project.

Fig.7.5.4 Child fallen into the bore well

Fig.7.5.5 Child is being raised from the bore well to the surface

2021-2025

BOREWELL RESCUE ROBOT

A

MAJOR PROJECT REPORT

of

Submitted in the Fulfilment of the requirements for the award of the Degree of

BACHELOR OF TECHNOLOGY

IN

ELECTRONICS AND COMMUNICATION ENGINEERING

Submitted by

B. Ashwitha	21R21A0408
G. Harshith	21R21A0423
K. Sridhar Reddy	21R21A0436
K. Vaishnavi	22R25A0404
M. Aditya	22R25A0405

UNDER THE GUIDANCE OF

Mrs. S. Monika

Assistant Professor

Department of ECE

A significant research project titled **"Design of a T-Slot Rectangular Microstrip Patch Antenna for 5G Applications at 28 GHz"** was developed using the ANSYS HFSS CoE. The project demonstrated the enhancement of antenna parameters such as gain, return loss, and bandwidth, proving its suitability for millimeter-wave 5G applications.

Published in IEEE:

Title: Millimeter Wave Range 'T' shaped slot antenna for 5G Applications
Authors: Kiran Chand Ravi, S V S Prasad, G KarthikReddy ,KayalaPavan Sai
Conference/Journal: IEEE [**2024 4th International Conference on Artificial Intelligence and Signal Processing (AISP)]**

DOI/Link:https://ieeexplore.ieee.org/abstract/document/10870822 (https://ieeexplore.ieee.org/abstract/document/10870822)

MATLAB Centre of excellence Lab:

Fig.7.5.6 MATLAB Centre of excellence Lab

1. Fig.7.5.6 shows the MATLAB Center of Excellence in the Department of Electronics and Communication Engineering. It is equipped with computers, a white marker board, air conditioners, an LCD projector, and a dedicated discussion room.
2. The systems are configured with Intel Dual Core Pentium CPU R5800 Processor, 8GB RAM, 500GB hard disk, and include a color printer with scanner to support research and academic activities.
3. This research center facilitates research for both students and faculty in fields such as communication and control systems, digital signal processing, image and video processing, and system modeling and simulation.
4. The lab provides an environment that promotes innovation, offering both the hardware and software tools needed for advanced research.
5. The overall ambiance of the laboratory is excellent, ensuring a conducive atmosphere for focused work and academic collaboration.

VLSI Centre of excellence Lab:

Fig.7.5.7 VLSI Centre of excellence Lab

1. Fig7.5.7 shows the VLSI Center of Excellence lab. Department of Electronics and Communication Engineering features a VLSI Center of Excellence equipped with computers, a white marker board, air conditioners, an LCD projector, and a dedicated discussion room.
2. The systems are configured with Intel Dual Core Pentium CPU R5800 Processor, 8GB RAM, 500GB hard disk, and a color printer with scanner to support research and academic work.
3. This research center is utilized by both students and faculty for conducting research in areas such as VLSI, analog circuits, digital circuits, and RF circuit modeling and simulation.
4. The lab provides a conducive environment for advanced research, equipped with the necessary tools and resources for design and simulation work.
5. The overall ambiance of the laboratory is excellent, ensuring an ideal space for focused research and collaboration.

LABVIEW Academy Lab:

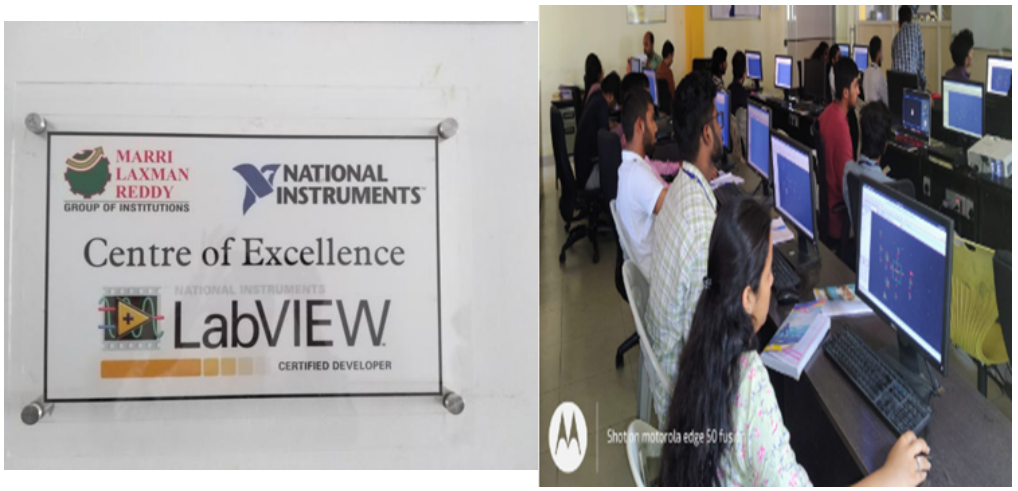


Fig.7.5.8 LABVIEW Academy Lab

1. Fig.7.5.8 shows the LabVIEW Academy lab .Department of Electronics and Communication Engineering houses a LabVIEW Academy, equipped with computers, a white marker board, air conditioners, an LCD projector, and a dedicated discussion room.
2. The systems are configured with Intel Dual Core Pentium CPU R5800 Processor, 8GB RAM, 500GB hard disk, and a color printer with scanner to facilitate research and academic work.
3. LabVIEW provides built-in support for NI hardware platforms such as MyDAQ and MyRIO, featuring device-specific blocks for these platforms, along with the Measurement and Automation Explorer (MAX) and Virtual Instrument Software Architecture (VISA) toolsets.

4. By integrating sensors with NI hardware for signal conditioning and utilizing LabVIEW software, students can build comprehensive measurement systems within a single platform.
5. These devices enable students to carry out projects related to signal processing and communication systems, providing hands-on experience in real-world applications.
6. The research center offers training and project opportunities in LabVIEW, supporting both students and faculty in carrying out research activities focused on signal processing and communication systems.
7. The overall ambiance of the laboratory is excellent, providing an ideal environment for research, learning, and collaboration.

Embedded and Robotics Centre of Excellency Lab:

Fig.7.5.9 Embedded and Robotics Centre of Excellency Lab

1. The Department of Electronics and Communication Engineering houses an Embedded Systems Lab, equipped with 30 computers, a white marker board, air conditioners, an LCD projector, and a dedicated discussion room.
2. The systems are configured with Intel Dual Core Pentium CPU R5800 Processor, 8GB RAM, 500GB hard disk, and a color printer with scanner to support research and academic activities. The lab is equipped with AtMega controllers and a variety of sensors, providing essential hardware for hands-on experimentation.
3. These devices enable students to work on projects related to embedded systems, allowing them to apply theoretical knowledge in practical, real-world applications.

The Centre of Excellence (CoE) serves as a dedicated facility for advanced learning, research, and innovation in emerging technologies. Equipped with state-of-the-art tools, simulation software, and hardware platforms, the CoE provides students with hands-on experience and a collaborative environment to work on real-time projects and societal challenges.

Students actively utilize the resources of the CoE to design, develop, and simulate systems in domains such as embedded systems, VLSI, RF and microwave engineering, robotics, and antenna design. The CoE fosters a research-oriented mind-set, enabling students to explore innovative solutions and build functional prototypes with academic and practical relevance.

As a result of these efforts, several student-led projects carried out in the CoE have led to the publication of technical papers in reputed national and international journals and conferences. These publications not only reflect the quality of research but also demonstrate the CoE's role in promoting academic excellence, technical skill development, and societal impact.

Proof of Utilization:

A noteworthy project titled **"Traffic Sign Recognition for Automated Speed Control Using Deep Learning"** was developed in the CoE. The research uses **MATLAB** for image processing to recognize traffic signs and control the speed of a robot chassis in real-time.

Published in IEEE:
Title: Traffic Sign Recognition for Automated Speed Control Using Deep Learning
Authors: Vijaya Kumar Velpula, SVS Prasad, JyothisriVadlamudi, SivaramakrishnaYechuri, Ganesh Miriyala, Manoj Kumar
Conference/Journal: IEEE [Recent Trends in Microelectronics, Automation, Computing and Communications Systems (ICMACC), International Conference]
DOI/Link:https://ieeexplore.ieee.org/abstract/document/10894397 (https://ieeexplore.ieee.org/abstract/document/10894397)

Industry-Institute Collaboration through MoUs for Job-Centric Learning

To strengthen industry-academia collaboration and bridge the gap between academic learning and industry expectations, the institution has signed several Memoranda of Understanding (MoUs) with leading companies and industrial organizations. These MoUs aim to train students in job-centric skills through hands-on exposure in Project Labs and Centers of Excellence (CoEs).

Under these agreements, students receive industry-oriented training in emerging domains such as VLSI, IoT, Embedded Systems, Artificial Intelligence, and RF Design. Industrial partners conduct expert sessions, workshops, and internship programs, enabling students to apply theoretical concepts in real-world scenarios. These partnerships also support final-year project development, promote innovation, and enhance employability by aligning student competencies with industry requirements.

The collaboration further encourages joint research, co-development of prototypes, and knowledge transfer through faculty development programs and guest lectures by industry professionals. These efforts collectively contribute to achieving the program outcomes and program-specific outcomes in a measurable and impactful manner.

Proof of Utilization – MoUs with Industry for Job-Centric Learning

To enhance employability and provide job-oriented training to students, the institution has established strategic partnerships with reputed industry organizations through signed Memoranda of Understanding (MoUs). These MoUs enable students to gain hands-on experience, industry exposure, and domain-specific skills using the resources available in Project Labs and Centers of Excellence (CoEs).

1. BSNL – RTTC Hyderabad

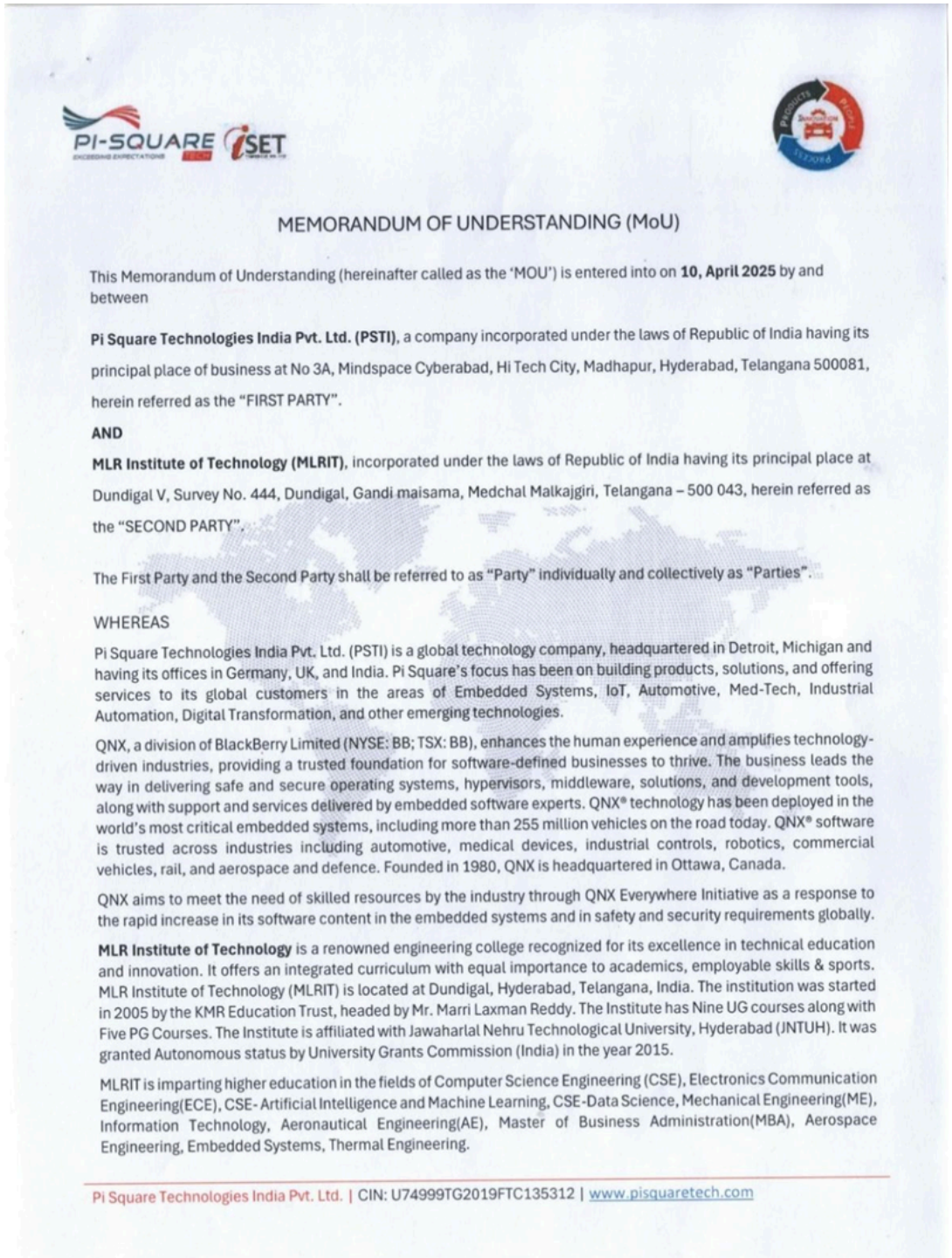
- **Purpose**: Industrial training in Telecommunications and IT Technologies
- **Utilization**: Students participate in internships, mini and major projects, and faculty development programs conducted by BSNL RTTC using real-time telecom infrastructure and IT tools.
- **Relevance**: Supports employability in core sectors through exposure to telecom standards, network systems, and ITU-compliant training.

2. Pi Square Technologies – QNX Program Partnership

- **Purpose:**
  To provide training and hands-on experience in embedded systems, safety-critical software development, and real-time operating systems (RTOS) through the QNX Everywhere initiative.
- **Utilization:**
  Students and faculty are trained in QNX Software Development Platform (QNX SDP) through certification programs, webinars, masterclasses, and project-based learning using real-world automotive, robotics, and industrial automation applications. Faculty members undergo

specialized training programs (FDPs), enabling them to mentor students in QNX-based projects and research. The QNX software tools and development platforms are utilized for student projects, research work, and hackathons organized within the Centre of Excellence (CoE) labs and project laboratories.

- **Relevance:**
  This collaboration strengthens students employability by equipping them with cutting-edge embedded and safety-critical software skills demanded by the automotive, healthcare, industrial automation, and aerospace sectors. It fosters research, innovation, and exposure to global industry standards, preparing students for core and product-based industries.



PI-SQUARE iSET

MEMORANDUM OF UNDERSTANDING (MoU)

This Memorandum of Understanding (hereinafter called as the 'MOU') is entered into on **10, April 2025** by and between

Pi Square Technologies India Pvt. Ltd. (PSTI), a company incorporated under the laws of Republic of India having its principal place of business at No 3A, Mindspace Cyberabad, Hi Tech City, Madhapur, Hyderabad, Telangana 500081, herein referred as the "FIRST PARTY".

AND

MLR Institute of Technology (MLRIT), incorporated under the laws of Republic of India having its principal place at Dundigal V, Survey No. 444, Dundigal, Gandi maisama, Medchal Malkajgiri, Telangana – 500 043, herein referred as the "SECOND PARTY".

The First Party and the Second Party shall be referred to as "Party" individually and collectively as "Parties".

WHEREAS

Pi Square Technologies India Pvt. Ltd. (PSTI) is a global technology company, headquartered in Detroit, Michigan and having its offices in Germany, UK, and India. Pi Square's focus has been on building products, solutions, and offering services to its global customers in the areas of Embedded Systems, IoT, Automotive, Med-Tech, Industrial Automation, Digital Transformation, and other emerging technologies.

QNX, a division of BlackBerry Limited (NYSE: BB; TSX: BB), enhances the human experience and amplifies technology-driven industries, providing a trusted foundation for software-defined businesses to thrive. The business leads the way in delivering safe and secure operating systems, hypervisors, middleware, solutions, and development tools, along with support and services delivered by embedded software experts. QNX® technology has been deployed in the world's most critical embedded systems, including more than 255 million vehicles on the road today. QNX® software is trusted across industries including automotive, medical devices, industrial controls, robotics, commercial vehicles, rail, and aerospace and defence. Founded in 1980, QNX is headquartered in Ottawa, Canada.

QNX aims to meet the need of skilled resources by the industry through QNX Everywhere Initiative as a response to the rapid increase in its software content in the embedded systems and in safety and security requirements globally.

MLR Institute of Technology is a renowned engineering college recognized for its excellence in technical education and innovation. It offers an integrated curriculum with equal importance to academics, employable skills & sports. MLR Institute of Technology (MLRIT) is located at Dundigal, Hyderabad, Telangana, India. The institution was started in 2005 by the KMR Education Trust, headed by Mr. Marri Laxman Reddy. The Institute has Nine UG courses along with Five PG Courses. The Institute is affiliated with Jawaharlal Nehru Technological University, Hyderabad (JNTUH). It was granted Autonomous status by University Grants Commission (India) in the year 2015.

MLRIT is imparting higher education in the fields of Computer Science Engineering (CSE), Electronics Communication Engineering(ECE), CSE- Artificial Intelligence and Machine Learning, CSE-Data Science, Mechanical Engineering(ME), Information Technology, Aeronautical Engineering(AE), Master of Business Administration(MBA), Aerospace Engineering, Embedded Systems, Thermal Engineering.

Fig.7.5.10 MoU of PiSquar

Relevance of LabVIEW Academy Lab to POs and PSOs:

The LabVIEW Academy Lab strongly supports the attainment of several Program Outcomes (POs) and Program Specific Outcomes (PSOs) by providing a platform for students to design, simulate, and implement projects in embedded systems and signal processing:

- **PO1 (Engineering Knowledge):** Students apply foundational knowledge of engineering, mathematics, and science while using LabVIEW tools for advanced system simulations and project development.
- **PO2 (Problem Analysis):** The lab facilitates the identification, formulation, and analysis of engineering problems through practical experimentation and project work.
- **PO3 (Design/Development of Solutions):** Students design customized hardware-software solutions for complex engineering problems using MyDAQ, MyRIO, and LabVIEW-based platforms.
- **PO4 (Conduct Investigations of Complex Problems):** Through simulation and experimentation, students investigate engineering problems, analyze data, and draw substantiated conclusions.
- **PO5 (Modern Tool Usage):** The lab promotes the use of modern engineering tools, specifically LabVIEW and National Instruments platforms, enhancing students proficiency in industry-relevant software.
- **PO8 (Individual and Team Work):** Students work individually and in teams on various research and mini-projects, promoting collaboration and leadership skills.
- **PO9 (Communication):** Students prepare project reports, documentation, and make presentations on their research work, strengthening communication skills.
- **PO11 (Life-long Learning):** The lab encourages independent learning and adaptability through exposure to new technologies and tools.

PSO1 (Proficiency in Specialized Tools): The LabVIEW Academy Lab significantly contributes to developing proficiency in specialized software tools essential for embedded system and VLSI design.

PSO2 (Technological Advancement in RF, Communication, and DSP): The use of LabVIEW for signal processing projects directly enhances the students' understanding of Digital Signal Processing (DSP) and related technologies.

Relevance of Embedded Systems and Robotics Lab to POs and PSOs: The Systems and Robotics Lab significantly contributes to the attainment of multiple Program Outcomes (POs) and Program Specific Outcomes (PSOs) by supporting students in embedded systems, robotics, and research-based projects:

- **PO1 (Engineering Knowledge):** Students apply core engineering concepts in mathematics, electronics, and embedded systems to develop and implement real-world robotic and control system applications.
- **PO2 (Problem Analysis):** Through practical problem-solving exercises, students Analyze complex system-level challenges and design effective robotic solutions.
- **PO3 (Design/Development of Solutions):** The lab fosters the design of innovative embedded and robotic systems that meet specified functional and societal needs.
- **PO4 (Conduct Investigations of Complex Problems):** Students use research-based methods to develop prototypes, perform experiments, collect data, and draw valid conclusions.
- **PO5 (Modern Tool Usage):** With licensed software tools and advanced computing systems, students are trained to use modern technologies for simulation, modeling, and system analysis.
- **PO8 (Individual and Team Work):** Students collaborate in multidisciplinary teams to develop research and innovation-based projects, building teamwork and leadership capabilities.
- **PO9 (Communication):** The preparation of research papers, project presentations, and technical reports enhances the students ability to communicate technical information effectively.
- **PO11 (Life-long Learning):** Students are encouraged to independently explore new technologies and approaches, promoting self-learning and continuous skill enhancement.

PSO1 (Proficiency in Specialized Tools): This lab provides students with expertise in using embedded system platforms, simulation software, and programming tools critical for robotics and system design.

PSO2 (Technological Advancement in RF, Communication, and DSP): Hands-on activities and projects using this labs resources help students strengthen their understanding of embedded system design, real-time control, and signal processing techniques, contributing to advancements in their field.

Relevance of ANSYS HFSS Lab to POs and PSOs: The ANSYS HFSS Lab plays a crucial role in supporting the attainment of various Program Outcomes (POs) and Program Specific Outcomes (PSOs) by enabling students to develop skills in RF, microwave engineering, and high-frequency electromagnetic analysis:

- **PO1 (Engineering Knowledge):** Students apply principles of electromagnetic theory, communication engineering, and high-frequency electronics to perform advanced simulations and solve engineering problems.
- **PO2 (Problem Analysis):** Through simulation-based projects, students identify, model, and analyze complex electromagnetic and RF-related challenges to propose effective solutions.
- **PO3 (Design/Development of Solutions):** Students design antennas, microwave circuits, and RF systems using HFSS software, considering practical and environmental constraints.
- **PO4 (Conduct Investigations of Complex Problems):** The lab enables students to simulate real-world RF problems, interpret simulation data, and synthesize findings into meaningful solutions.
- **PO5 (Modern Tool Usage):** Students gain proficiency in using ANSYS HFSS, an industry-standard electromagnetic simulation tool, thus enhancing their technological skills for real-world applications.
- **PO6 (The Engineer and Society):** Through the design of antennas and RF devices, students develop an understanding of societal applications such as communication systems, satellite technology, and healthcare devices.
- **PO8 (Individual and Team Work):** Students work individually and collaboratively on HFSS-based research projects, promoting teamwork and leadership skills.
- **PO9 (Communication):** Students present their project findings through reports, research papers, and seminars, enhancing their technical communication skills.
- **PO11 (Life-long Learning):** Exposure to cutting-edge RF simulation tools motivates students to continuously update their skills and stay abreast of technological advancements.

PSO1 (Proficiency in Specialized Tools): The lab enhances student expertise in specialized simulation tools like ANSYS HFSS, crucial for high-frequency and electromagnetic system design.

PSO2 (Technological Advancement in RF, Communication, and DSP): Students develop deep technical knowledge in RF and microwave engineering, strengthening their research capabilities and contributing to technological advancement through projects and publications.

Relevance of Cadence Lab to POs and PSOs: The Cadence Lab significantly contributes to achieving the Program Outcomes (POs) and Program Specific Outcomes (PSOs) by providing an advanced platform for digital system design, FPGA development, and research in electronics and embedded systems:

- **PO1 (Engineering Knowledge):** Students apply core concepts of electronics, digital design, and embedded systems to design and implement complex circuits using industry-standard tools like Cadence, Xilinx ISE, and Vivado.
- **PO2 (Problem Analysis):** Students identify design challenges, formulate strategies, and analyze outcomes while working on FPGA-based and SoC-based projects.
- **PO3 (Design/Development of Solutions):** The lab supports the design and development of optimized digital systems and embedded applications tailored to specific needs, considering technical and real-world constraints.
- **PO4 (Conduct Investigations of Complex Problems):** Students utilize simulation and hardware testing to investigate design effectiveness, perform data analysis, and validate solutions.
- **PO5 (Modern Tool Usage):** Students acquire proficiency in advanced electronic design automation (EDA) tools like Cadence and Vivado Design Suite, as well as hands-on experience with FPGA/CPLD kits and ZYNQ boards.
- **PO8 (Individual and Team Work):** Students collaborate in teams to develop projects, fostering leadership, coordination, and collaborative problem-solving skills.
- **PO09 (Communication):** Students document design processes, simulation results, and project outcomes effectively through technical reports and presentations.
- **PO10 (Project Management and Finance):** Students learn project planning, resource management, and cost considerations while handling real-world design and implementation tasks.
- **PO11 (Life-long Learning):** Exposure to rapidly evolving VLSI and embedded system technologies encourages students to engage in continual skill development.

PSO1 (Proficiency in Specialized Tools): The lab provides extensive training on professional tools like Cadence, Xilinx, and Vivado, building strong technical skills for careers in VLSI and embedded system industries.

PSO2 (Technological Advancement in RF, Communication, and DSP): The use of advanced FPGA and SoC platforms aids students in developing communication system modules and digital signal processing projects, strengthening their competency in these domains.Top of FormBottom of Form

PART E: First Year faculty and financial Resources

(Data to be filled in for the first year course faculty and budget allocation and utilization)

E1. First Year Student-Faculty Ratio (FYSFR)

Table No. E1.1: FYSFR details.

Year	Sanctioned intake of all UG programs (S4)	No. of required faculty (RF4= S4/20)	No. of faculty members in Basic Science Courses & Humanities and Social Sciences including Management courses (NS1)	No. of faculty members in Engineering Science Courses (NS2)	Percentage= No. of faculty members ((NS1*0.8) + (NS2*0.2))/(No. of required faculty (RF4)); Percentage= ((NS1*0.8) +(NS2*0.2))/RF
2022-23(CAYm2)	1320	66	50	15	65
2023-24(CAYm1)	1440	72	58	19	70
2024-25(CAY)	1020	51	58	21	99

E2. Budget Allocation, Utilization, and Public Accounting at Institute Level

Table No. E2.1: Budget and actual expenditure incurred at Institute level.

Items	Budgeted in 2024-2025	Actual Expenses in 2024-2025 till	Budgeted in 2023-2024	Actual Expenses in 2023-2024 till	Budgeted in 2022-2023	Actual Expenses in 2022-2023 till	Budgeted in 2021-2022	Actual Expenses in 2021-2022 till
Infrastructure Built-Up	7500000	7574506	9000000	8594884	117000000	115980277	50000000	49352618
Library	1900000	1849230	3000000	2839275	2400000	2385029	4100000	4037917
Laboratory equipment	10500000	10219503	24500000	24444761	28500000	28129329	25500000	25173922
Teaching and non-teaching staff salary	350000000	345020998	350000000	330938647	207500000	206774402	255000000	250938539
Outreach Programs	830000	808552	830000	826839	780000	773949	720000	712543
R&D	14500000	14206905	12000000	11740304	5500000	5238455	4000000	3946389
Training, Placement and Industry linkage	6000000	5517732	9200000	9041809	5000000	4820897	4200000	4194012
SDGs	500000	495627	170000	167471	420000	412896	230000	224377
Entrepreneurship	360000	358265	1000000	996986	930000	925537	2200000	2129530
Others, specify	177910000	174323811	190300000	185251428	191970000	182044553	204050000	197371341
Total	**570000000**	**560375129**	**600000000**	**574842404**	**560000000**	**547485324**	**550000000**	**538081188**

E3. Budget Allocation, Utilization, and Public Accounting at Program Specific Level

Table No. E3.1: Budget and actual expenditure incurred at program level.

Items	Budgeted in 2024-2025	Actual Expenses in 2024-2025 till	Budgeted in 2023-2024	Actual Expenses in 2023-2024 till	Budgeted in 2022-2023	Actual Expenses in 2022-2023 till	Budgeted in 2021-2022	Actual Expenses in 2021-2022 till
Laboratory equipment	570000.00	556175.00	1900000.00	1852816.00	950000.00	931714.00	4000000.00	3885462.00

Software	0	0	0	0	800000.00	799079.00	0	0
SDGs	0	0	0	0	0	0	0	0
Support for faculty development	160000.00	151250.00	650000.00	620165.00	600000.00	549899.00	500000.00	473605.00
R & D	1450000.00	1443233.00	1800000.00	1777334.00	800000.00	747769.00	1500000.00	1508853.00
Industrial Training, Industry expert, Internship	1300000.00	1298290.00	1700000.00	1662135.00	900000.00	876527.00	800000.00	762548.00
Miscellaneous Expenses*	350000.00	343324.00	2200000.00	2177488.00	900000.00	881352.00	2500000.00	2430599.00
Total	**3830000.00**	**3792272.00**	**8250000.00**	**8089938.00**	**4950000.00**	**4786340.00**	**9300000.00**	**9061067.00**